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## PRACTICAL ASPECTS OF OPERATING AND ANALYTICAL RELIABILITY ASSESSMENT OF FPGA-BASED I&C SYSTEMS

*Operating reliability assessment of instrumentation and control systems (I&Cs) is always one of the most important activities, especially for critical domains such as nuclear power plants (NPPs). It is an important source of I&C reliability information preferable to lab testing data because it provides information on I&C reliability under real use conditions. That is the reason that now it is a common practice for companies to have an established process of collecting operating reliability data on a large variety of used components on regular basis, maintaining a database with failure information, total operation time, typical failure modes, etc. The intensive use of complicated components like field-programmable gate arrays (FPGAs) in I&C which appear in upgrades and newly-built nuclear power plants makes the task to develop and validate advanced operating reliability assessment methods that consider specific technology features very topical. Increased integration densities make the reliability of integrated circuits the most crucial point in modern NPP I&Cs. Moreover, FPGAs differ in some significant ways from other integrated circuits: they are shipped as blanks and are very dependent on the design configured into them. Furthermore, FPGA design could be changed during planned NPP outage for different reasons. Considering all possible failure modes of FPGA-based NPP instrumentation and control systems at the design stage is a quite challenging task. Therefore, operating reliability assessment is one of the most preferable ways to perform a comprehensive analysis of FPGA-based NPP I&Cs. Based on information in the literature and own experience, operational vs analytical reliability could be pretty far apart. For that reason, analytical reliability assessment using reliability block diagrams (RBD), failure modes, effects and diagnostics analysis (FMEDA), fault tree analysis (FTA), fault insertion testing (FIT), and other techniques and their combinations are important to meet requirements for such systems. The paper summarizes our experience in operating and analytical reliability assessment of FPGA based NPP I&Cs.*

**Keywords:** *reliability analysis; reliability block diagrams; failure modes, effects, and diagnostics analysis.*

### Introduction

For analytical reliability assessments Markov chain models, Reliability block diagrams (RBD) and Fault trees analysis (FTA) are typically used. Traditionally, application of such methods has been rather straightforward. However, with the implementation of modern I&Cs, there is no common practice on how to use them. In addition, challenges of application of such methods for complex systems like FPGA-based NPP I&Cs lie in fact that assessments are based on assumptions the influence of which on the results may be underestimated and not well understood.

Operating reliability assessment is used for verifying and completing analytical assessment. We compare results that were obtained by analytical calculations with results obtained from operation and propose unified reliability assessment approach.

In FPGA-based systems, a high-level design is implemented with the configurable logic blocks made available by a given FPGA chip. In order to attain a realistic model and satisfactory accuracy of the analysis,

we propose to represent FPGA-based system at this implementation level.

There are a lot of reliability assessment techniques during development and operation stages described by standards MIL [1], IEEE [2], IEC [3] and industrial guides [4]. These techniques can be combined to analyze reliability and evaluate quantitative indicators [5]. Particularities of reliability and safety assessment for FPGA-based I&C are analyzed in [6].

Objective of the paper is to summarize experience on operating reliability analysis of FPGA based NPP I&Cs. In Section 2 we provide overview of analytical and operational reliability assessment methods used at RPC Radiy. Sections 3 and 4 provide details on operating and analytical assessments respectively. The results we obtained illustrate the proposed approach can assess the reliability of the FPGA-based NPP I&Cs reasonably. It also allows performing verification of obtained results by possibility of different methods usage.

In Section 5 we provide details on Failure Modes, Effects and Diagnostics Analysis for FPGA-based I&Cs and discuss the importance of tool support for operating

reliability assessment that obviously cannot be overemphasized.

Finally, in Sections 6 and 7 we provide an assessment case study and conclusions including future research directions.

## 1. Reliability Assessment of FPGA-based NPP I&C Systems: Approach

Reliability assessment activities are critical for maintaining system and customers' reliabilities during operation of FPGA-based NPP I&C systems. Reliability assessment typically covers both analytical and operational reliability assessment. RPC Radiy's approach is shown on Figure 1 (FMEDA – Failure Modes, Effects and Diagnostics Analysis, RBD - Reliability Block Diagrams, CCFA - Common Cause Failure Analysis, FTA - Fault Tree Analysis, HAZOP - Hazardous Operations).

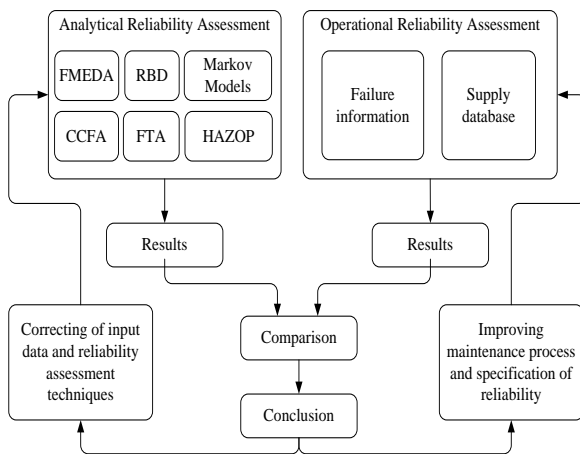


Fig. 1. RPC Radiy's reliability assessment flow

Results obtained by analytical and operational assessments are being compared, and then conclusions are made, providing feedback for possibility of improvement of maintenance process (customer side) and reliability assessment techniques (I&C system supplier side).

During reliability assessment a lot of reliability data is being processed. Figure 2 provides classification of data sources, basic reliability data (obtained from field)

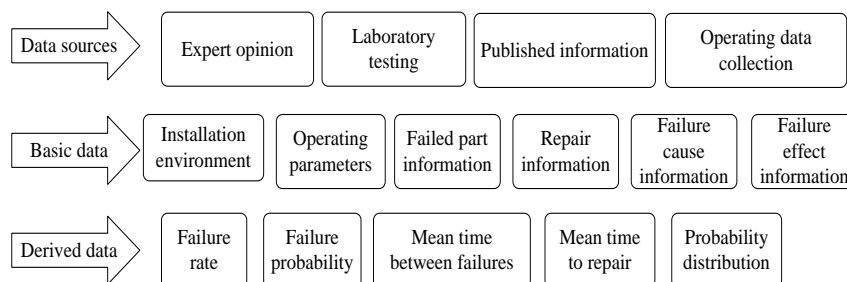


Fig. 2. Reliability data

and derived reliability data (obtained after performed calculations on basic data).

Thus, the approach is based on combining of the different techniques and data to assess and prove trustworthiness of the assessment results.

## 2. Operating Reliability Assessment

Reliability data on supplied I&C systems is collected from RPC Radiy customers on regular basis, not less than once in a quarter. Such information includes failure data that is used to calculate operational reliability and can be used for further improvements.

Figure 3 shows toolbox used at RPC Radiy during operating reliability assessment.

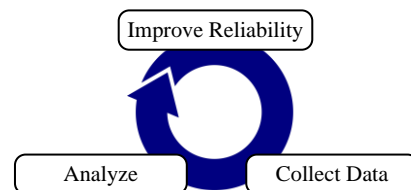


Fig. 3. RPC Radiy's toolbox for operating reliability assessment

During analysis stage the following actions are performed:

- classification of source information by accepted features (operating conditions, type of failed components etc);
- identification of components that reduce the product reliability;
- identification of failure causes;
- efficiency estimation of design-engineering and (or) organizational measures;
- estimation of reliability indices and statistical data processing;
- data processing about usage of spare parts;
- comparison of obtained data with analytical results;
- analysis and classification of data about components failures;



Basing on formulas (1) and (2) the following expression for failure rate can be obtained:

$$\lambda_{\text{sys}}(t) = \sum_{k=1}^n \lambda_k(t), \quad (3)$$

where  $\lambda_k$  – failure rate of k-th element,  
n – number of elements in system.

## 4. Failure Modes, Effects and Diagnostics Analysis

### 4.1. Standards

FMEA is a systematic way to identify and evaluate the effects of different component failure modes, to determine what could eliminate or reduce the chance of failure, and to document the system in consideration. FMEDA (Failure Mode Effect and Diagnostic Analysis) is an extension of FMEA that combines standard FMEA techniques with the extension to identify automatic diagnostic techniques and the failure modes relevant to safety instrumented system design.

It is a technique recommended to generate failure rates for each important category (safe detected, safe undetected, dangerous detected, dangerous undetected, fail high, fail low, etc.) in the safety models. The format for the FMEDA is an extension of the standard FMEA format from MIL STD 1629A [1]. The FMEDAs are consistent the FMEA guidance of IEEE Std 352-2016 [2], Sections 4.5.2 and 5.2.

The failure rate data used for the FMEDAs are from the Electrical and Mechanical Component Reliability Handbook [4], which was derived using over ten billion unit operational hours of field failure data from multiple sources and failure data from various databases.

The rates were chosen in a way that is appropriate for safety integrity level verification calculations. It is expected that the actual number of field failures due to random events will be less than the number predicted by these failure rates. For hardware assessment according to IEC 61508 [3], only random equipment failures are of interest. It is assumed that the equipment has been properly selected for the application and is adequately commissioned such that early life failures may be excluded from the analysis.

### 4.2. FPGA Failures

The methods used to estimate the reliability of RadICS (FPGA-based I&C platform produced by RPC Radiy) Modules that are installed in a rack are based on the Electrical and Mechanical Component Reliability

Handbook instead of MIL HDBK 217F [10], which is recommended in IEEE Std 352-2016 [2]. The Electrical and Mechanical Component Reliability Handbook provides more current data for modern electronic hardware than MIL HDBK 217F. The FMEDA for each RadICS Module considered the different groups of components that affected module functionality. The following groupings were evaluated:

Common	The portion of the RadICS Module that is always used.
Input	The portion of the RadICS Module used by one on-board input channel.
Output	The portion of the RadICS Module used by one on-board output channel.
LVDS	The portion of the logic module providing communication to one input/output module via low-voltage differential signaling.

The following definitions for the failure of the device were considered in order to judge the failure behavior of the RadICS Modules:

Fail-Safe State	State where all discrete outputs are de-energized.
Fail-Safe	Failure that causes the device to go to the defined fail-safe state without a demand from the process. (abbreviation: S).
Fail-Safe Detected	Failure that is detected by automatic self-diagnostics, which causes the output signal to go to the predefined fail-safe state (i.e., output modules de-energized). (abbreviation: SD).
Fail-Safe Undetected	Failure that is safe and that is not diagnosed by automatic self-diagnostics. (abbreviation: SU).
Fail Dangerous	Failure that does not respond to a demand from the process (i.e., being unable to go to the defined fail-safe state).
Analog Input	Failure that deviates the measured input value by more than 2 % of span and leaves the value within active scale.
Fail Dangerous Detected	Failure that is dangerous but is detected by automatic diagnostics. (abbreviation: DD).
Fail Dangerous Undetected	Failure that is dangerous and that is not being diagnosed by automatic diagnostics. (abbreviation: DU).
No Effect	Failure of a component that is part of the safety function but that has no effect on the safety function. (abbreviation: NE) It is important to realize that the No Effect failures are no longer included in the Safe Undetected failure category according to IEC 61508:2010.

Annunciati on Detected	Failure that does not directly impact safety but does impact the ability to detect a future fault (e.g., a fault in a diagnostic circuit) and that is detected by internal diagnostics. A Fail Annunciation Detected failure leads to a false diagnostic alarm. This condition leads to maintenance, and if the safety channel is not shut down (put into the safe state) during this maintenance, the time must be accounted for in any system level reliability calculation. (abbreviation: AD).
Annuncia-tion Undetected	Failure that does not directly impact safety but does impact the ability to detect a future fault (e.g., a fault in a diagnostic circuit) and that is not detected by internal diagnostics. AU failures are treated as No Effect failures for Safe Failure Fraction calculation. (abbreviation: AU).
Fail Dangerous Undetected after Sur-veillance Test	Failure that is dangerous and that is not being diagnosed by either automatic diagnostics or the periodic surveillance test. (abbreviation: DUaPT).

The failure categories listed above expand on the categories listed in IEC 61508:2010 [3], which are only safe and dangerous, both detected and undetected. Under IEC 61508:2010, the No Effect failures cannot contribute to the failure rate of the safety function.

The Annunciation failures are provided for those who wish to do reliability modeling more detailed than required by IEC 61508:2010. It is assumed that the probability model will correctly account for the Annunciation failures; otherwise the Annunciation Undetected failures have to be classified as Dangerous Undetected failures according to IEC 61508:2010 (worst-case assumption).

### 4.3. FPGA Failure Modes

FPGA-based systems are analyzed on different implementation level. For example, in [7] failure taxonomy is provided for system level, division level, I&C unit level, I&C module level, while in [8] failure modes are provided for FPGA itself. In order to attain a realistic model and satisfactory accuracy of the analysis, we propose to represent FPGA-based system at the following implementation level: configurable logic blocks made available by a given FPGA chip.

The following failure modes could be considered:

- MUX select;
- Programmable Interconnect Points (PIP) short;
- PIP open;
- buffer off;
- buffer on;
- Lookup Table(LUT) value change;
- control bit change;
- user flip-flop;
- block random access memory (RAM);
- half-latches;
- power network.

### 4.4. Tool Support

Reliability assessment complexity necessitates development of software tools that assist plant personnel and vendor engineers to manage reliability assessment activities and can provide solutions to various decision making issues.

As was discussed in [9], the following is to be considered during selection of software package:

- types of data input (graphically, as a plain text, in a matrix form etc);
- export (import) features;
- supported analysis methods;
- embedded feature of reports generation.

At RPC Radiy we use our own developed tool called AXMEA (Figure 6). So far it supports only FMEDA, but adding other methods and techniques to it is in progress.

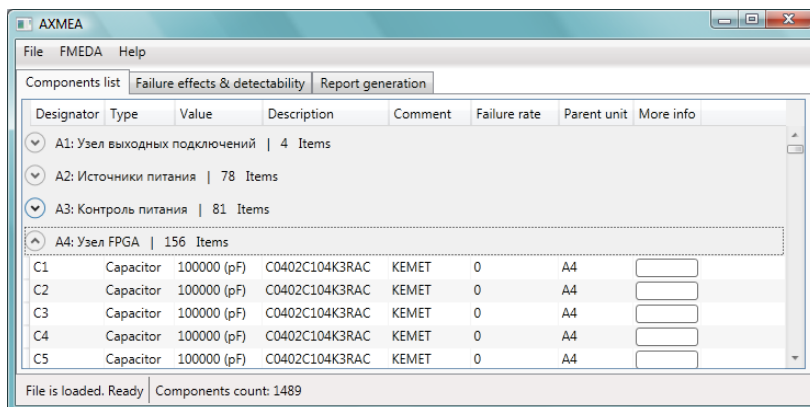


Fig. 6. AXMEA Tool

For operational reliability assessment is a spreadsheet-based tool is used (Figure 7). This tool summarizes data on all I&Cs supplied by RPC Radiy, providing information on system, module and component level.

I&C	3AEC						PAEC				SAS3C		IOV			IOV	
	Unit 1	Unit 2	Unit 3	Unit 4	Unit 5	Unit 6	Unit 1	Unit 2	Unit 3	Unit 4	Unit 1	Unit 2	Unit 1	Unit 2	Unit 3	Unit 5	Unit 6
RTS(main)	3-1 RTS	3-2 RTS	3-3 RTS	3-4 RTS	3-5 RTS	3-6 RTS			P-3 A3-IT3	P-4 A3-IT3	X-1 A3-IT3	X-2 A3-IT3	IOV-1 A3-IT3	IOV-2 A3-IT3	IOV-3 A3-IT3		
RTS(div)	3-1 A3-IT3	3-2 A3-IT3	3-3 A3-IT3	3-4 A3-IT3	3-5 A3-IT3	3-6 A3-IT3			P-3 A3-IT3	P-4 A3-IT3	X-1 A3-IT3	X-2 A3-IT3	IOV-1 A3-IT3	IOV-2 A3-IT3	IOV-3 A3-IT3		
RTS (main)							P-1 A3	P-2 A3									
RTS (div)							P-1 A3 (L)	P-2 A3 (R)									
RPCLS	3-1 APM	3-2 APM	3-3 APM				P-1 APM	P-2 APM	P-3 APM	P-4 APM	X-1 APM	X-2 APM	IOV-1 APM	IOV-2 APM			
Nuclear Island							P-1 CH9 PO	P-2 CH9 PO					IOV-1 CH9 PO	IOV-2 CH9 PO			
Turbine Island							P-2 CH9 TO	P-3 CH9 TO					IOV-1 CH9 TO				
ESFAS-1							P-1 YCB-1	P-2 YCB-1					IOV-1 YCB-1	IOV-2 YCB-1		K-5 YCB-1	K-6 YCB-1
ESFAS-2							P-1 YCB-2	P-2 YCB-2					IOV-1 YCB-2	IOV-2 YCB-2		K-5 YCB-2	K-6 YCB-2
ESFAS-3							P-1 YCB-3	P-2 YCB-3					IOV-1 YCB-3	IOV-2 YCB-3		K-5 YCB-3	K-6 YCB-3
ACMS																	
RCS													IOV-1 CTBY				
ICS																	

Fig. 7. Spreadsheet for Operating Reliability Assessment

### 5. Case Study

As an example we take Speed Measuring Device, which block diagram is shown on Figure 8.

Speed Measuring Device includes the following blocks:

- Variable Reluctance Speed Sensor (A0);
- DC/DC converters (A1, A7);
- Variable Reluctance Speed Sensor interface device (A2);
- optocouplers (A3, A5, A8);
- AC/DC converter (A4);
- logic solver (A6);
- output converters (A9);

- relay (A10).

Blocks A3 and A10 are used only to switch device into testing mode and are not used during normal device operation, therefore they are not taken into reliability analysis.

Figure 9 shows reliability block diagram for Speed Measuring Device. Since block A7 is identical to block A1, and block A8 to A5, they are shown on reliability block diagram as 2\*A1 and 2\*A5 accordingly.

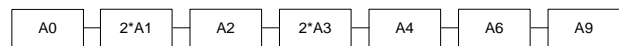


Fig. 9. Reliability Block Diagram of Speed Measuring Device

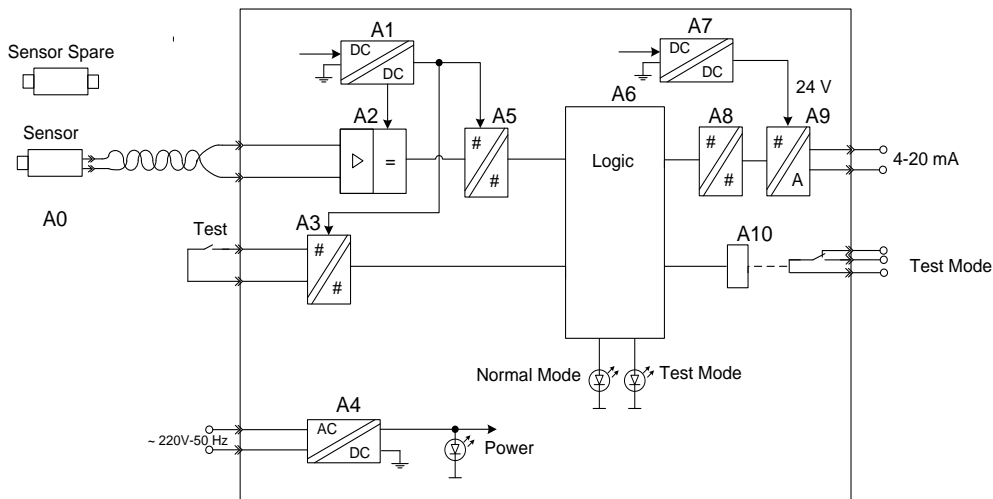


Fig. 8. Block Diagram of Speed Measuring Device



Failure rates for blocks A1-A9 were obtained from supplier documentation. For A0 failure rate MIL-217F [10] was used. The failure rate for this component is defined as:

$$\lambda_p = \lambda_B \pi_T \pi_Q \pi_E / 10^6, \quad (4)$$

Table 1 provides values required for calculation.

Table 1

Values for A0 failure rate calculation

Parameter	Value	Comments
$\lambda_B$	0.000050/10 <sup>6</sup>	Assumed variable inductor (MIL-HDBK-217F [10], Section 11.2)
$\pi_T$	3.5	Operation should not exceed +150°C T <sub>HS</sub> used +150°C (MIL-HDBK-217F [10], Section 11.2)
$\pi_Q$	3.0	Commercial component (MIL-HDBK-217F [10], Section 11.2)
$\pi_E$	6.0	Assumed "Ground Fixed" environment (MIL-HDBK-217F [10], Section 11.2)

Calculated failure rate of A0 is 3.15E-09.

Table 2 summarizes failures rates for all blocks.

Table 2

Failure rates

No.	Block	Part Type	Quantity of Parts	Failure Rate	Data Origin
1.	A0	VRS SENSOR	1	3.15E-09	MIL-HDBK-217F
2.	A1	DC/DC	2	2.23E-07	recom-international.com
3.	A2	AMPL	1	2.24E-08	maximintegrated.com
4.	A3	OPTO	2	1.39E-07	avagotech.com
5.	A4	AC/DC	1	2.78E-06	recom-international.com
6.	A6	FPGA	1	2.98E-07	intel.com
7.	A9	DAC	1	1.43E-09	analog.com

Failure rate of Speed Measuring Device is 3.82898 E-06, and mean time between failures is 261166 hours.

### Conclusions

In this paper we have introduced approach to assessment of FPGA-based NPP I&C systems which was implemented by RPC Radiy during last ten years. It is based on combining of the techniques of operational and analytical calculation and assessment of the systems. The most interesting and important points of this approach are renewing of the data for operational assessment and possibilities of comparing results using different techniques and different combinations of the techniques chains.

The future steps will be dedicated to development reliability assessment environment for NPP I&C systems using commercial off-the-shelf and RPC Radiy tools.

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## ПРАКТИЧНІ АСПЕКТИ ОПЕРАЦІЙНОГО ТА АНАЛІТИЧНОГО ОЦІНЮВАННЯ НАДІЙНОСТІ ІУС НА ПЛІС

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Оцінювання експлуатаційної надійності інформаційно-управляючих систем (ІУС) є одним з найбільш важливих напрямків діяльності, особливо в критичних областях, таких як атомні електростанції (АЕС). Вона є важливим джерелом інформації щодо надійності ІУС, кращим, ніж дані, отримані за результатами лабораторних випробувань, оскільки надає інформацію про надійність ІУС в реальних умовах використання. Тому у теперішній час для компаній стало звичайною практикою впроваджувати процес збору даних з експлуатаційної надійності на великій кількості використовуваних компонентів на регулярній основі, підтримувати базу даних з інформацією про відмови, сумарним напрацюванням, типовими видами відмов і т.д.

Інтенсивне використання складних компонентів, таких як програмовані логічні інтегральні схеми (ПЛІС) у модернізованих і у новозбудованих АЕС, робить дуже актуальним завдання розроблення та затвердження передових методів оцінювання експлуатаційної надійності, що враховують особливості конкретних технологій. Висока щільність інтеграції призводить до того, що надійність інтегральних схем стає найбільш важливою характеристикою сучасних ІУС АЕС. Більш того, ПЛІС істотно відрізняються від інших інтегральних схем: вони поставляються в вигляді заготовок і сильно залежать від створеної в них конфігурації. Крім того, конфігурація ПЛІС може через змінюватися під час планового відключення АЕС з різних причин. Урахування всіх можливих відмов ІУС на ПЛІС на етапі проектування – достатньо складне завдання. Таким чином, оцінювання експлуатаційної надійності є одним з найбільш затребуваних способів проведення комплексного аналізу ІУС на ПЛІС. Аналіз літературних джерел і власний досвід показали, що експлуатаційна надійність може істотно відрізнятися від аналітичної. З цієї причини аналітичне оцінювання надійності з використанням структурних схем надійності (RBD), аналізу видів, наслідків і діагностованості відмов (FMEDA), аналізу дерева відмов (FTA), тестування засівом дефектів (FIT) та інших методів і їх комбінацій, є важливим для відповідності вимогам, що пред'являються до таких систем. У даній статті узагальнено наш досвід аналізу експлуатаційної надійності ІУС на ПЛІС.

**Ключові слова:** аналіз надійності; структурні схеми надійності; аналіз видів, наслідків та діагностованості відмов.



**ПРАКТИЧЕСКИЕ АСПЕКТЫ ОПЕРАЦИОННОГО И АНАЛИТИЧЕСКОГО ОЦЕНИВАНИЯ НАДЕЖНОСТИ ИУС НА ПЛИС***Е. В. Бабешко, В. С. Харченко, К. П. Леонтиев, Е. В. Ручков*

Оценка эксплуатационной надежности информационно-управляющих систем (ИУС) является одним из наиболее важных направлений деятельности, особенно в критических областях, таких как атомные электростанции (АЭС). Она является важным источником информации о надежности ИУС, более предпочтительным, чем данные, полученные по результатам лабораторных испытаний, поскольку предоставляет информацию о надежности ИУС в реальных условиях использования. Поэтому в настоящее время для компаний стало обычной практикой внедрять процесс сбора данных об эксплуатационной надежности на большом количестве используемых компонентов на регулярной основе, поддерживать базу данных с информацией об отказах, суммарной наработкой, типовыми видами отказов и т.д.

Интенсивное использование сложных компонентов, таких как программируемые логические интегральные схемы (ПЛИС) в модернизируемых и во вновь построенных АЭС, делает очень актуальной задачу разработки и валидации передовых методов оценки эксплуатационной надежности, которые учитывают особенности конкретных технологий. Высокая плотность интеграции приводит к тому, что надежность интегральных схем становится наиболее важной характеристикой современных ИУС АЭС. Более того, ПЛИС существенно отличаются от других интегральных схем: они поставляются в виде заготовок и сильно зависят от созданной в них конфигурации. Кроме того, конфигурация ПЛИС может изменяться во время планового отключения АЭС по разным причинам. Учет всех возможных отказов ИУС на ПЛИС на этапе проектирования - довольно сложная задача. Таким образом, оценка эксплуатационной надежности является одним из наиболее предпочтительных способов проведения комплексного анализа ИУС на ПЛИС. Анализ литературных источников и собственный опыт показали, что эксплуатационная надежность может существенно отличаться от аналитической. По этой причине аналитическая оценка надежности с использованием структурных схем надежности (RBD), анализа видов, последствий и диагностируемости отказов (FMEDA), анализа дерева отказов (FTA), тестирования засевом дефектов (FIT) и других методов и их комбинаций, является важным для соответствия требованиям, предъявляемым к таким системам. В данной статье обобщен наш опыт анализа эксплуатационной надежности ИУС на ПЛИС.

**Ключевые слова:** анализ надежности; структурные схемы надежности; анализ видов, последствий и диагностируемости отказов.

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